Amendments to the Abstract

Please **amend** the Abstract to read.

-- The amount of jitter incurred when reading data written into a FIFO ~~(12)~~ can be reduced by clocking the FIFO with Read Clock pulses at a frequency $x f_n$ where x is a whole integer and f_n is the frequency at which the memory is clocked to write data. Read Addresses are applied to the FIFO at a frequency on the order of f_n to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations. The duration of at least one successive Read Addresses is altered in response to memory usage status to maintain memory capacity below a prescribed threshold.--